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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/611,395	06/30/2003	Shriram Ramanathan	42P16666	1525
8791 7590 03/26/2008 BLAKELY SOKOLOFF TAYLOR & ZAFMAN 1279 OAKMEAD PARKWAY SUNNYVALE, CA 94085-4040				
EXAMINER RODGERS, COLLEEN E				
ART UNIT 2813		PAPER NUMBER		
MAIL DATE 03/26/2008		DELIVERY MODE PAPER		

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

### Office Action Summary

**Application No.**

10/611,395

**Applicant(s)**

RAMANATHAN ET AL.

**Examiner**

Colleen E. Rodgers

**Art Unit**

2813

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 03 January 2008.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-5 and 7-12 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 1-5 and 7-12 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO-8508)  
Paper No(s)/Mail Date \_\_\_\_\_  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_  
5) ☐ Notice of Informal Patent Application  
6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. This Office Action responds to the Amendment filed 3 January 2008. By this amendment, claims 1 and 12 are amended and claims 13-20 and 22-27 are canceled. Claims 1-5 and 7-12 remain pending.

#### *Claim Rejections - 35 USC § 102*

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 4, 8, 10 and 11 are rejected under 35 U.S.C. 102(b) as being anticipated by **Shibata et al** (US Patent Application Publication 2002/0031904).

Regarding claim 1, **Shibata et al** disclose a method comprising:

providing a first wafer **1** having a number of conductors **11** disposed on a surface thereof;

providing a second wafer **2** having a number of conductors **21** disposed on a surface thereof;

depositing a layer **11a** of a metal only on each of the conductors disposed on the surface of the first wafer such that the conductors disposed on the surface of the second wafer do not have a metal layer deposited thereon [see Fig. 2; see also paragraph 0046];

aligning the first wafer with the second wafer;

physically contacting the metal layer on each of the conductors of the first wafer with a mating one of the conductors on the second wafer; and

forming a bond between the metal layer on each of the conductors of the first wafer and the mating one conductor of the second wafer, wherein all regions of the first and second wafer surfaces

surrounding the mating conductors remain unbonded, wherein the bond is formed at a temperature between approximately 100 and 300 degrees Celsius [see paragraph 0044].

Regarding claim 4, **Shibata et al** disclose the method of claim 1, furthermore wherein the conductors 11 of the first wafer 1 comprise copper [see paragraph 0041].

Regarding claim 8, **Shibata et al** disclose the method of claim 1, furthermore wherein depositing the layer of metal on each of the conductors of the first wafer comprises selectively depositing the metal on each of the conductors [see Fig. 2; see also paragraph 0044].

Regarding claim 10, **Shibata et al** disclose the method of claim 1, furthermore wherein the metal layer on each of the conductors of the first wafer comprises a number of islands [see Fig. 2].

Regarding claim 11, **Shibata et al** disclose the method of claim 10, furthermore wherein the islands are selectively deposited on each of the conductors of the first wafer [see Fig. 2; see also paragraph 0044].

#### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Shibata et al** (US Patent Application Publication 2002/0031904) in view of **Tong et al** (US Patent Application Publication 2004/0157407). **Shibata et al** disclose the method of claim 1, but do not disclose that, prior to depositing the metal layer on each of the conductors of the first wafer, dielectric material

(i.e., a native oxide as required by claim 3) is removed from the surface of the first wafer (specifically the conductors, again as required by claim 3). **Tong et al** teach a method of bonding in a similar manner, using the same materials (namely, copper). Furthermore, **Tong et al** teach that sputter cleaning and evaporation are employed to remove a dielectric material, namely a native oxide, from the surface of the wafer, specifically from the conductors [see paragraph 0075]. It would have been obvious to one of ordinary skill in the art at the time of invention to clean native oxide from the surfaces of the metals to be bonded in order to reduce contact resistance.

6. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Shibata et al** (US Patent Application Publication 2002/0031904) in view of **Zuniga-Ortiz et al** (US Patent Application Publication 2003/0141593). Regarding claim 5, **Shibata et al** disclose the method of claim 1. **Shibata et al** disclose that the metal **11a** exemplarily comprises Sn, but also teaches that "the materials are not limited to ... Sn" [see paragraph 0045]. **Zuniga-Ortiz et al** teach a similar wafer bonding process wherein a metal **207** is formed on conductors, wherein the metal is formed of gold, palladium, platinum, silver and alloys thereof [see paragraph 0070]. It would have been obvious to one of ordinary skill in the art at the time of invention to use the metal materials of **Zuniga-Ortiz et al** in the method taught by **Shibata et al** because **Zuniga-Ortiz et al** teach that these materials are exceptionally bondable [see paragraph 0070 and 0071].

7. Claims 7 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over **Shibata et al** (US Patent Application Publication 2002/0031904) in view of **Mirkin et al** (US Patent Application Publication 2004/0226464).

Regarding claim 7, **Shibata et al** disclose the method of claim 1. **Shibata et al** do not disclose wherein depositing the layer of metal on each of the conductors of the first wafer comprises forming a blanket layer of metal on each of the conductors of the first wafer and removing the metal from at least portions of the first wafer surface. **Mirkin et al** teach a method of bonding wafers, wherein a metal layer **132** is formed over a conductor **126** on a first wafer **120**. Furthermore, **Mirkin et al** teach wherein the metal layer is formed by forming a blanket layer of material and removing the metal from at least portions of the first wafer surfaces [see paragraph 0044]. It would have been obvious to one of ordinary skill in the art at the time of invention to use the method of **Mirkin et al** in the process taught by **Shibata et al** because it is well known in the art to form a blanket layer and pattern it in order to arrive at an island configuration.

Regarding claim 12, **Shibata et al** disclose a method comprising:  
providing a first wafer **1** having a number of conductors **11** disposed on a surface thereof;  
providing a second wafer **2** having a number of conductors **21** disposed on a surface thereof;  
depositing a layer **11a** of a metal only on each of the conductors disposed on the surface of the first wafer such that the conductors disposed on the surface of the second wafer do not have a metal layer deposited thereon [see Fig. 2; see also paragraph 0046];

aligning the first wafer with the second wafer;  
physically contacting the metal layer on each of the conductors of the first wafer with a mating one of the conductors on the second wafer; and  
forming a bond between the metal layer on each of the conductors of the first wafer and the mating one conductor of the second wafer, wherein all regions of the first and second wafer surfaces surrounding the mating conductors remain unbonded [see paragraph 0044],

wherein the metal layer on each of the conductors of the first wafer comprises a number of islands [see Fig. 2].

**Shibata et al** do not disclose wherein the islands are formed by a process comprising depositing a blanket layer of the metal over the conductors and the surface of the first wafer and removing the blanket metal layer from at least portions of the first wafer surface and from portions of each conductor to form the number of islands on each conductor. **Mirkin et al** teach a method of bonding wafers, wherein a metal layer **132** is formed over a conductor **126** on a first wafer **120**. Furthermore, **Mirkin et al** teach wherein the metal layer is formed by forming a blanket layer of material and removing the metal from at least portions of the first wafer surfaces [see paragraph 0044]. It would have been obvious to one of ordinary skill in the art at the time of invention to use the method of **Mirkin et al** in the process taught by **Shibata et al** because it is well known in the art to form a blanket layer and pattern it in order to arrive at an island configuration.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over **Shibata et al** (US Patent Application Publication 2002/0031904) in view of **Neuhaus et al** (US Patent Application Publication 2002/0027294). **Shibata et al** disclose the method of claim 8, but do not disclose wherein selectively depositing the metal on each of the conductors of the first wafer comprises an electroless plating process, an electroplating process or a contact displacement plating process. **Neuhaus et al** disclose a method of performing metal-metal bonding for semiconductor wafers comprising electroplating a number of metallic islands to a metallized contact [see paragraph 0027-0028, 0038 and 0073]. It would have been obvious to one of ordinary skill in the art at the time of invention to use the method of **Neuhaus et al** in the method of **Shibata et al** because **Neuhaus et al** teach that this method eliminates several manufacturing steps, which simplifies the process for

component assembly. Furthermore, it provides improved electrical performance, particularly lower metal-to-metal contact resistance [see paragraph 0021].

### ***Response to Arguments***

9. Applicant's arguments with respect to claims 1-5 and 7-12 have been considered but are moot in view of the new ground(s) of rejection.

### ***Conclusion***

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Colleen E. Rodgers whose telephone number is (571) 272-8603. The examiner can normally be reached on Monday through Friday, 8:00 AM to 5:00 PM.



If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Carl Whitehead Jr./  
Supervisory Patent Examiner, Art Unit 2813

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Examiner, Art Unit 2813